CONDUANT

HSS-8324-DSP PCI EXPRESS HIGH SPEED OPTICAL FPGA BOARD

Product Features

- AMD (Xilinx) XCKU115 FPGA with 5520 DSP slices
- PCI Express single slot compatible
- 8-lane PCI Express Gen 3.0 (max 8 GBps) backplane interface
- 24 High-Speed Serial (HSS) lanes (48 fibers or 24 copper differential pairs), up to 16.3 Gbps line rates:
  - Dual 12-lane, 850 nm MPO/MTP optical ports (24 lanes total)
  - Four QSFP ports (16 lanes total)
- 2 banks of 4GiB DDR3 SDRAM (8GiB total)
- 8 MiB QDR II+ SRAM
- Clock generation with integer and fractional divide
- Xilinx eFUSE or battery-backed 256-bit AES bitstream encryption
- UART interface (3 wire, RS-232 compatible)
- 4 PCIe back panel-accessible user-configurable MMCX connectors for triggers or clocks
- 8 internal user programmable LEDs
- 1 Gib configuration flash
- Power and FPGA configuration status LEDs
- JTAG interface for flash and FPGA access
- Xilinx power/temperature system monitor

CE

Specifications

Form Factor	PCI Express single or double slot (depending on HSS connector option)
High Speed Serial (HSS)	24 lanes with line rates up to 16.3 Gbps each
HSS Connection Options	Dual MTP/MPO 12 lane/24 fiber connectors using Samtec Firefly modules (1 PCIe slot) 4x QSFP ports, user provided or specified modules (2 PCIe slots)
Additional External Connectors	4x MMCX for clock, trigger, or other signal IO
Dimensions	10.0" (D) x 0.627" (W) x 4.2" (H)
Weight	1 lb (0.5 kg)
DRAM	8 GiB DDR3 SDRAM 2x512Mx64b @ 932 MHz
SRAM	8 MiB QDR II+ Extreme SRAM 4Mx18b @ 632 MHz
Clock Generation	Skyworks clock generator with integer and fractional divide
Power	Typical 35W*

**Power will vary depending on user programming and clock speeds*

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Available Xilinx FPGA Options

Kintex Ultrascale XCKU115		
	System Logic Cells	1,451,100
	CLB Flip Flops	1,326,720
	CLB LUTs	663,660
	Distributed RAM	18.3 Mb
	Block RAM	76.9 Mb
	DSP Slices	5,250
Kintex Ultrascale XCKU085		
	System Logic Cells	1,088,325
	CLB Flip Flops	995,040
	CLB LUTs	497,520
	Distributed RAM	13.4 Mb
	Block RAM	56.9 Mb
	DSP Slices	4,100

Provided Vivado Project includes:

- VHDL source code for board self-test which can also be used as a programming examples on how to access different IP Core ports:
  - Independent DRAM self test, one for each bank
  - SRAM self test
  - HSS Interface loopback test, one port sends data, another port receives and verifies data
- VHDL source code that instantiates Vivado cores, available signals, and pins to expose all available resources that the user can then connect to with their own IP (Intellectual Property) as desired:
  - One PCI Express Gen3 8-lane Core
  - Two 4GiB DDR3 DRAM MIG Cores
  - One 8MiB QDRII+ SRAM MIG Core
  - One System Monitor to monitor board voltages
  - Two 12-lane HSS (High-Speed-Serial) instances implemented as either Aurora or ODI per user request
- External signals exposed include:
  - Four MMCX front panel connectors
  - 8 LEDs on back of board

Included Windows/Linux Software:

- Program to flash FPGA code updates over the PCIe bus

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Advanced Capabilities

The Conduant HSS-8324 FPGA board provides a user programmable hardware platform that is able to sustain full-duplex high-bandwidth transfers through its 8-lane Gen3 PCI Express interface and its two 12-lane HSS interfaces while performing complex calculations. The PCIe interface provides a theoretical maximum throughput of 8 GBps (simultaneous in and out) while each HSS port (12 lanes up to 16 Gbps per lane) supports a full duplex transfer at theoretical rates over 190 Gbps.

The board includes both 8 GiB of high-speed DDR3 SDRAM and 8 MiB of QDR II+ SRAM. At the center of the design is an AMD (Xilinx) Kintex Ultrascale FPGA which interconnects all ports and other devices while supplying additional resources within the FPGA. This particular FPGA contains a high count of DSP elements which uniquely suits this board for signal processing.

With up to 24 HSS lanes and 4 MMCX coaxial connections available, the board can be used for numerous applications that require high speed data connectivity with advanced DSP functionality. Note that each HSS lane can operate independently or in a bonded configuration if supported by the protocol being used. Popular HSS protocols that can be implemented include but are not restricted to Aurora, Interlaken, Serial FPDP and ODI (Optical Data Interface) with optical or copper connectivity.

At power-on, the FPGA is quickly configured with the user program by the SPI x4 serial flash memory device. This provides the fast wake-up required for PCI Express. The user content can be encrypted with a key that is programmed in the FPGA in non-volatile EFUSEs or can be preserved in volatile memory so long as the on-board battery is not removed. This feature makes this product particularly attractive for applications in which protecting the FPGA intellectual property from cloning or reverse engineering is important.

To improve clocking flexibility, the board includes a Skyworks Si5341B part that supports both integer and fractional divides. While the provided VHDL project uses the internal I2C bus to initialize these clocks at power-up for the self test function, the user can access the I2C bus if different frequencies are needed.

Other models of Kintex or Virtex Ultrascale FPGAs may be available. Check with your Conduant sales representative.

Warranty & Customer Support

Conduant hardware products are backed by a limited one-year warranty. All software includes a 90 day warranty. Maintenance and priority support is available on a yearly subscription basis. Please contact your Conduant sales representative for more details.

Customer support is provided through a comprehensive web portal at www.conduant.com/support. Private logins and trouble ticket management are provided along with technical downloads, knowledge base, and other support tools.

Options

FPGA options | *contact Conduant for availability*
High speed serial | *MPO/MTP 850 nm fiber, Four QSFP*
Battery backup for encrypted FPGA configuration support
Custom software | *Contact your Conduant sales representative for custom software availability*

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