CONDUANT

HSS-8324-DSP PXI EXPRESS HIGH SPEED OPTICAL FPGA BOARD

Product Features

- AMD XCKU115 or XCKU085 FPGA
- Up to 5520 FPGA DSP slices
- PXIe single slot compatible
- 8-lane PCI Express Gen 3.0 (max 8 GBps)
- 24 High-Speed Serial lanes (48 fibers) supporting up to 16.3 Gbps lanes.
- Dual MPO optical ports (24 fiber, 850nm)
- 8 GB DDR3 SDRAM memory
- 8 MB QDR II+ SRAM memory
- Fraction divide clock synthesis
- 4x MMCX connectors

Advanced Capabilities

The Conduant HSS-8324-DSP FPGA board provides a hardware platform that is able to sustain high-bandwidth transfers through its 8-lane Gen3 PXI Express (PXIe) interface and its two 12-lane HSS interfaces while performing complex calculations. The PXIe interface provides a theoretical maximum throughput of 8 GBps while each HSS port (12 lanes up to 16.3 Gbps per lane) supports full duplex transfer at theoretical rates over 190 Gbps.

The FPGA is an AMD Kintex Ultrascale XCKU115 or XCKU085 which interconnects all ports and devices while supplying additional resources within the FPGA. The board includes both 8 GiB of high-speed DDR3 SDRAM and 8 MiB of QDR II+ SRAM.

With 24 High-Speed Serial (HSS) lanes and 4 MMCX coaxial connections available, the board can be used for numerous applications that require high speed data connectivity with advanced DSP functionality. Note that each HSS lane can operate independently or in a bonded configuration depending on the the protocol being used. Popular HSS protocols include AMD Aurora, Interlaken, Serial FPDP, and ODI.

The FPGA is quickly configured with the user program by the SPI x4 serial flash memory device. This provides the fast wake-up required for PCI Express enumeration. The user code can be encrypted with a key in the FPGA non-volatile EFUSEs or in volatile memory using the on-board battery. This makes the board suitable for applications that require protecting the FPGA intellectual property.

The board includes a Skyworks clock synthesis part that supports both integer and fractional divides. The internal I2C bus can be used to initialize these clocks.

www.conduant.com
sales@conduant.com
1.303.485.2721
1.888.497.7327 *toll free*

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Specifications

FPGA	AMD Kintex Ultrascale XCKU115 or XCKU085
Encryption	AMD eFuse or battery-backed 256-bit AES bitstream
PXI Express Revision	1.0 ECN 1
PXIe Backplane	PCIe Gen3 x8 (8 GB/s) PXI signals (triggers, clocks, etc.)
Form Factor	PXI Express hybrid, peripheral or timing slot
High Speed Serial (HSS)	24 lanes with line rates up to 16.3 Gbps each
HSS Connectors	Dual MTP/MPO 12 lane/24 fiber connectors using Samtec Firefly modules
Additional External Connectors	4x MMCX 50 Ω for clock, trigger, or other signal IO JTAG for AMD programinng or debug
Clock Generation	Skyworks clock generator with integer and fractional divide
Dimensions	6.1875" (D) x 0.787" (W) x 5.0" (H)
Weight	< 1 lb (0.5 kg)
DRAM	8 GiB DDR3 SDRAM 2x512Mx64b @ 932 MHz
SRAM	8 MiB QDR II+ Extreme SRAM 4Mx18b @ 632 MHz
Clock Generation	Skyworks clock generator with integer and fractional divide
IO Interface	UART Interface (3 wire, RS232 compatible)
User programmable LEDs	Dual front panel, 8 internal (back of board)
Flash memory	Micron 1 GiB configuration flash (SPI 4 bits)

Available AMD FPGA Options

Kintex Ultrascale XCKU115		
	System Logic Cells	1,451,100
	CLB Flip Flops	1,326,720
	CLB LUTs	663,660
	Distributed RAM	18.3 Mb
	Block RAM	76.9 Mb
	DSP Slices	5,250
Kintex Ultrascale XCKU085		
	System Logic Cells	1,088,325
	CLB Flip Flops	995,040
	CLB LUTs	497,520
	Distributed RAM	13.4 Mb
	Block RAM	56.9 Mb
	DSP Slices	4,100

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FPGA Software

Provided AMD Vivado Project includes:

- VHDL source code for board self-test which can also be used as a programming examples on how to access different IP Core ports:
  - Independent DRAM self test, one for each bank
  - SRAM self test
  - HSS Interface loopback test, one port sends data, another port receives and verifies data
- VHDL source code that instantiates Vivado cores, available signals, and pins to expose all available resources that the user can then connect to with their own IP (Intellectual Property) as desired:
  - One PCI Express Gen3 8-lane Core
  - Two 4GiB DDR3 DRAM MIG Cores
  - One 8MiB QDRII+ SRAM MIG Core
  - One System Monitor to monitor board voltages
  - Two 12-lane HSS (High-Speed-Serial) instances implemented as either Aurora or ODI per user request
- External signals exposed include:
  - Four MMCX front panel connectors
  - Two front panel LEDs
  - 8 LEDs on back of board

Available Windows Software:

- Windows Driver
- Program to read/write registers and flash FPGA code updates over the PCIe bus

Warranty & Customer Support

Conduant hardware products are backed by a limited one-year warranty. All software includes a 90 day warranty. Maintenance and priority support is available on a yearly subscription basis. Please contact your Conduant sales representative for more details.

Customer support is provided through a comprehensive web portal at www.conduant.com/support. Private logins and trouble ticket management are provided along with technical downloads, knowledge base, and other support tools.

Options

FPGA options | *contact Conduant for availability*
High speed serial | *MPO/MTP 850 nm fiber, Four QSFP*
Battery backup for encrypted FPGA configuration support
Custom software | *Contact your Conduant sales representative for custom software availability*

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